EDVANTA

Ignite your growth, inspire your mind

PROFESSIONAL CERTIFICATE PROGRAM

VLSI Design

A 12-Week Industry-Ready Online Course

From logic gates to silicon — master the complete VLSI design flow with hands-on projects, live mentoring, and real-world industry alignment. Built for early professionals, graduate students, and career-transitioners ready to break into one of the most in-demand fields in semiconductor engineering.

12 Weeks Structured learning across 3 progressive phases	**Weekend Sessions** Recorded concepts + live 1:1 mentoring every week
Industry-Aligned Tools, workflows, and real-world scenarios	**Project-Based** Mini projects and assignments every phase

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

COURSE OVERVIEW

Why VLSI — And Why Now?

The global semiconductor market is projected to exceed **$1 trillion by 2030**. VLSI design sits at the heart of every chip powering AI accelerators, 5G modems, automotive systems, and consumer electronics. Demand for skilled VLSI engineers far outpaces supply — and companies are actively seeking professionals who can hit the ground running.

Explosive Market Demand

Global chipmakers — TSMC, Intel, AMD, Qualcomm — are expanding design teams aggressively. VLSI roles consistently rank among the highest-paid engineering positions worldwide.

Skill Gap Is Real

Most graduates lack hands-on EDA tool experience. This course bridges the gap between academic theory and the practical workflows hiring managers actually expect.

Career Acceleration

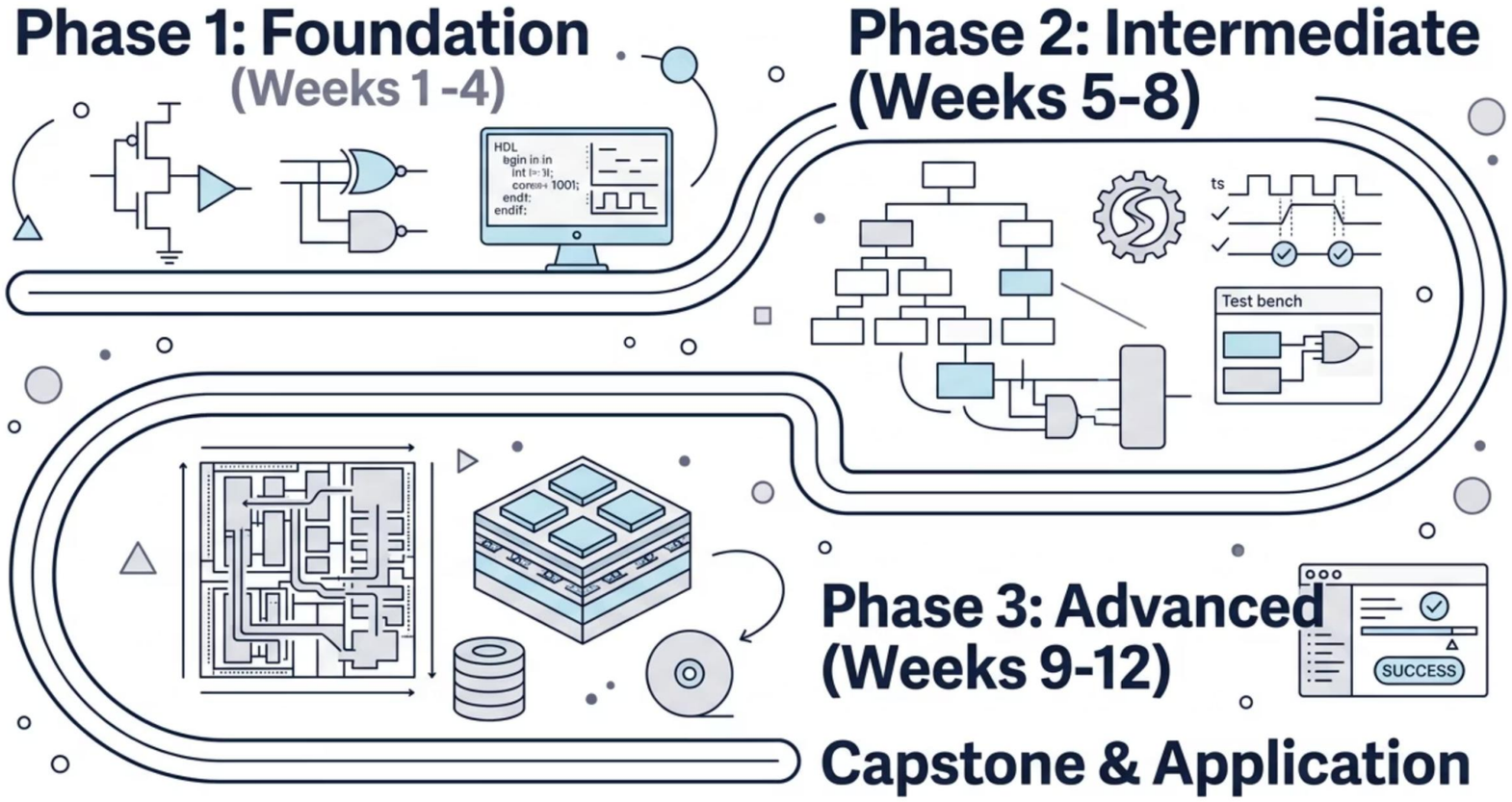
Whether you're targeting RTL design, physical design, verification, or analog layout — this program gives you a structured, portfolio-ready pathway into the industry.

EDVANTA

PROGRAM ARCHITECTURE

How the Course Is Structured

Every week follows a consistent, two-part format: a **weekend recorded session** covering core concepts with demonstrations, followed by a **live mentoring session** for doubt-clearing, case discussions, and personalized feedback. The 12-week program is divided into three progressive phases.



Weekly Format

- Recorded concept session (2–3 hrs)
- Live 1:1 or small-group mentoring (1 hr)
- Practical exercise + assignment

Content Mix

- 70–80% core concepts and fundamentals
- 10–15% industry use cases and applications
- 10% tools, EDA workflows, and demos

EDVANTA

Ignite your growth, inspire your mind

PHASE 1 — FOUNDATION

Weeks 1–4: Building Strong Fundamentals

The foundation phase ensures every learner starts from a common, solid baseline — regardless of their background. You will build intuition for how transistors work, how logic is expressed in hardware description languages, and how simulation tools are used to verify basic designs before synthesis.

1

Week 1 — CMOS & Device Physics

- MOSFET structure and operation (nMOS/pMOS)
- CMOS inverter: static and dynamic behavior
- Propagation delay, power dissipation basics
- Intro to SPICE simulation (LTspice/NgSPICE)
- Hands-on: Simulate a CMOS inverter DC sweep

2

Week 2 — Digital Design Fundamentals

- Boolean algebra, minimization (Karnaugh maps)
- Combinational circuits: MUX, decoder, adder
- Sequential circuits: flip-flops, latches, FSMs
- Timing: setup, hold, clock-to-Q concepts
- Hands-on: Design a 4-bit ripple carry adder

3

Week 3 — HDL Coding with Verilog

- RTL vs. behavioral vs. structural modeling
- Verilog syntax: modules, ports, always blocks
- Testbench writing and waveform analysis
- Simulation with ModelSim or Vivado Simulator
- Hands-on: Code and verify a 4-bit ALU in Verilog

4

Week 4 — Logic Synthesis Intro + Phase Project

- RTL-to-gate synthesis concepts
- Liberty files, standard cell libraries
- Synthesis constraints: area, timing, power
- Tool intro: Synopsys Design Compiler (DC) / Yosys
- Mini Project: Design and synthesize a UART transmitter

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

PHASE 1 — LEARNING OUTCOMES

What You'll Achieve by Week 4

1

Device Intuition

Understand MOSFET operation and CMOS circuit behavior at a practical level

2

Digital Fluency

Design and analyze combinational and sequential logic circuits confidently

3

HDL Proficiency

Write synthesizable Verilog RTL and validate designs using testbenches

4

Synthesis Ready

Run a basic synthesis flow and interpret area/timing reports from EDA tools

Phase 1 Assignment: Complete a fully verified UART transmitter in Verilog, synthesized with area and timing reports. Submit waveforms, schematic, and a written reflection on design trade-offs.

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

PHASE 2 — INTERMEDIATE

Weeks 5–8: RTL, Verification & Timing

Phase 2 deepens your design skills and introduces the industry-standard flows used by professional engineers daily. You will learn how to write clean, optimized RTL, close timing, build structured verification environments, and understand power intent — skills that directly map to RTL Engineer and Design Verification Engineer job descriptions.

1

Week 5 — Advanced RTL Design

- RTL coding guidelines and synthesis-friendly constructs
- Pipeline design: stages, hazards, forwarding
- Clock domain crossing (CDC) basics
- Design reuse and parameterized modules
- Hands-on: Build a 3-stage pipelined processor core

2

Week 6 — Static Timing Analysis (STA)

- Setup and hold timing paths explained
- SDC constraints: clock definition, exceptions
- Timing reports: slack, WNS, TNS interpretation
- Tool: Synopsys PrimeTime or OpenSTA
- Hands-on: Analyze and fix timing violations in a sample design

3

Week 7 — Functional Verification

- Verification planning: coverage goals and testplan
- SystemVerilog basics: interfaces, classes, assertions
- UVM methodology overview (testbench architecture)
- Code coverage vs. functional coverage
- Hands-on: Write a directed and constrained-random testbench for a FIFO

4

Week 8 — Power Analysis + Phase Project

- Dynamic vs. static power dissipation
- UPF/CPF: power domains, isolation, retention cells
- Low-power design techniques: clock gating, multi-Vt
- Tool: Synopsys PrimeRail / Cadence Voltus (overview)
- Mini Project: STA closure and power analysis of a synthesized RISC-V core

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

PHASE 2 — LEARNING OUTCOMES

What You'll Achieve by Week 8

🔧 RTL Excellence

Write clean, synthesizable, timing-aware RTL code following industry coding standards

⏱️ Timing Closure

Read and fix setup/hold violations using SDC constraints and STA tool reports

✅ Verification Skills

Build structured testbenches in SystemVerilog and understand UVM-based verification flows

⚡ Power Awareness

Apply low-power techniques and interpret power reports — a critical skill in mobile and IoT chip design

Phase 2 Assignment: Perform STA closure and power analysis on an open-source RISC-V core (e.g., PicoRV32). Document violations found, fixes applied, and power summary. Peer-reviewed submission.

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

PHASE 3 — ADVANCED

Weeks 9–12: Physical Design & Tapeout Flow

Phase 3 takes you from gate-level netlist to a manufacturable chip layout. This is where VLSI becomes tangible — you will run a complete physical design flow, perform sign-off checks, and understand how designs go from RTL to real silicon. The capstone project ties every skill together into a portfolio-ready deliverable.

1

Week 9 — Floorplanning & Placement

- Chip floorplan: die area, aspect ratio, utilization
- I/O ring, power grid, and macro placement
- Standard cell placement algorithms and optimization
- Tool: Cadence Innovus / OpenROAD
- Hands-on: Floorplan and place a synthesized UART design

2

Week 10 — Clock Tree Synthesis & Routing

- Clock tree goals: skew, latency, insertion delay
- CTS algorithms: H-tree, balanced buffering
- Global routing vs. detailed routing fundamentals
- Routing DRC: spacing, width, via rules
- Hands-on: Run CTS and routing on your placed design

3

Week 11 — Physical Verification

- DRC: design rule checking concepts and violation types
- LVS: layout vs. schematic — netlist comparison
- ERC, antenna rule checks
- Sign-off tools: Mentor Calibre / Synopsys IC Validator
- Hands-on: Run DRC/LVS clean on a standard cell layout block

4

Week 12 — Tapeout Flow + Capstone

- GDSII generation and layer mapping
- Sign-off checklist: STA, power, DRC/LVS, ERC
- Tapeout handoff: foundry requirements overview
- Open-source flow: OpenLane for end-to-end practice
- Capstone: Full RTL-to-GDSII flow on a custom design

EDVANTA

PHASE 3 — LEARNING OUTCOMES

What You'll Achieve by Week 12

Floorplan & Placement

Create a manufacturable chip floorplan with proper power grid and macro placement

CTS & Routing

Execute clock tree synthesis and detailed routing meeting timing and DRC targets

Physical Sign-Off

Run and resolve DRC/LVS checks using industry-standard verification tools

Tapeout Ready

Generate GDSII and understand the complete sign-off checklist before a chip goes to fab

Capstone Project: Complete RTL-to-GDSII flow on a custom digital design (e.g., 8-bit CPU or SPI controller) using OpenLane + PDK. Deliverables include: netlist, placed-and-routed layout, DRC/LVS clean report, timing summary, and a 5-minute recorded demo presentation.

EDVANTA

Ignite your growth, inspire your mind

INDUSTRY EXAMPLES

Industry Example #1: Timing Closure at a Mobile SoC Startup

The Business Problem

A fabless mobile SoC startup was preparing their first 5G modem chip for tapeout at TSMC 7nm. Post-synthesis STA reports showed 200+ setup violations across the critical data path, threatening the tapeout schedule by 3 weeks — a costly delay given customer commitments.

The Role of Early Professionals

Junior RTL and physical design engineers were tasked with triaging violation categories, re-running synthesis with tightened constraints, and iterating on clock domain crossing fixes under senior guidance.

How VLSI Concepts Applied

- SDC constraint refinement to accurately model clock uncertainty
- Retiming and pipeline insertion to reduce critical path depth
- Multi-corner multi-mode (MCMM) STA to catch worst-case paths
- Physical optimization (useful skew, buffer upsizing) in Innovus

Tools Used

Synopsys Design Compiler, Cadence Innovus, PrimeTime, internal scripts (Python/Tcl)

Measurable Impact

All critical paths closed within 5 days. Tapeout proceeded on schedule, saving an estimated **$180K** in delay costs. The team's STA methodology was adopted as the company standard.

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

INDUSTRY EXAMPLES

Industry Example #2: DRC/LVS Clean at an ASIC Design House

The Business Problem

An ASIC design services company won a contract to deliver a custom power management IC (PMIC) for an industrial IoT client. Physical verification revealed 1,400+ DRC violations and 12 LVS mismatches just 6 weeks before the agreed tapeout date — a critical milestone tied to contract payment.

The Role of Early Professionals

Junior physical design engineers ran automated DRC waiver scripts, manually resolved antenna violations on metal layers, and debugged LVS mismatches in the power domain — directly supervised by a senior layout lead.

How VLSI Concepts Applied

- Layer-by-layer DRC triage using Mentor Calibre runsets
- Antenna diode insertion to fix long-wire antenna violations
- LVS netlist debugging: identifying missing ties and floating gates
- ERC checks to ensure no electrical rule errors in power domains

Tools Used

Mentor Calibre DRC/LVS, Cadence Virtuoso, SKILL scripting for batch corrections

Measurable Impact

DRC/LVS clean achieved 4 days before tapeout. Client received the GDSII on time. The junior engineers' scripting work reduced DRC cycle time by **40%** on subsequent projects.

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

INDUSTRY EXAMPLES

Industry Example #3: UVM Verification of an AI Inference Accelerator

The Business Problem

A semiconductor company developing a custom AI inference chip needed to verify a 256-wide systolic array — a complex datapath block for matrix multiplication. Manual directed testing was insufficient; the team needed to achieve >95% functional coverage before synthesis freeze.

The Role of Early Professionals

Graduate-level verification engineers built constrained-random test sequences, developed coverage models, and debugged assertion failures in the systolic array control logic — gaining direct exposure to production UVM methodology.

How VLSI Concepts Applied

- UVM agent, scoreboard, and coverage collector architecture
- SystemVerilog Assertions (SVA) for protocol compliance checks
- Constrained-random stimulus to cover corner-case weight loading
- Functional coverage closure: 97.3% achieved across all bins

Tools Used

Cadence Xcelium (simulation), Cadence vManager (coverage), Synopsys VCS, internal Python regression harness

Measurable Impact

3 critical RTL bugs caught pre-synthesis, saving an estimated **2–3 weeks** of post-synthesis debug. The coverage methodology was reused for the full chip-level verification campaign.

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

TOOLS & TECHNOLOGY STACK

EDA Tools & Platforms You'll Use

Industry relevance requires hands-on exposure to the actual tools used by professional engineers. This course covers both **industry-standard commercial tools** (for understanding and awareness) and **open-source equivalents** (for hands-on practice throughout the program).

🔬 Simulation

- ModelSim / QuestaSim
- Cadence Xcelium
- Synopsys VCS
- LTspice / NgSPICE
- *Open-source:* Icarus Verilog, GHDL

⚙️ Synthesis

- Synopsys Design Compiler
- Cadence Genus
- *Open-source:* Yosys
- Xilinx Vivado (FPGA prototyping)
- Liberty (.lib) file comprehension

📐 Physical Design

- Cadence Innovus
- Synopsys IC Compiler II
- *Open-source:* OpenROAD, OpenLane
- Cadence Virtuoso (analog layout)
- Magic VLSI layout tool

✅ Sign-Off & Verification

- Synopsys PrimeTime (STA)
- Mentor Calibre (DRC/LVS)
- Synopsys IC Validator
- *Open-source:* OpenSTA, KLayout
- Cadence vManager (coverage)

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

CAREER ALIGNMENT

Job Roles This Course Prepares You For

VLSI is a broad field with several distinct career tracks. This course is designed to give you a strong enough foundation to target entry-level and junior roles across the full spectrum — and to specialize deeper once placed.

RTL Design Engineer

Write and optimize synthesizable RTL in Verilog/SystemVerilog. Work on datapaths, control logic, and IP blocks for SoCs. Common at Qualcomm, MediaTek, Apple Silicon, Intel.

Design Verification Engineer (DV)

Build UVM testbenches, write assertions, close coverage. One of the most in-demand roles in the industry — often 2 DV engineers per RTL designer. Common at all major semiconductor companies.

Physical Design Engineer

Run floorplan, placement, CTS, and routing flows. Ensure timing closure and DRC/LVS clean sign-off. Common at ASIC design houses, foundry partners, and fabless companies.

FPGA / Prototyping Engineer

Implement and verify ASIC designs on FPGA platforms for early software bring-up. Uses Vivado, Quartus, and custom bring-up scripts. Common at networking and AI chip companies.

CAD / EDA Support Engineer

Maintain EDA tool environments, write flows in Python/Tcl, and support design teams with automation. Great entry role for those who enjoy scripting and infrastructure.

Mixed-Signal / Analog Layout Engineer

Create precision analog circuit layouts in Virtuoso. Requires understanding of device matching, shielding, and layout-dependent effects. Common in analog IP companies and foundries.

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

SKILLS PROGRESSION

Skills Map: Beginner → Job Ready

The course is designed as a deliberate skill escalation — each phase builds directly on the last, ensuring you reach job-readiness by Week 12. Use this map to self-assess your current position and track your growth throughout the program.

Skill Domain	Beginner (Wk 1–4)	Intermediate (Wk 5–8)	Job Ready (Wk 9–12)
Digital Design	Boolean logic, flip-flops, FSMs	Pipelining, CDC, design reuse	Full RTL block design with constraints
HDL / Coding	Basic Verilog modules + testbenches	SystemVerilog, interfaces, assertions	UVM testbench architecture
Synthesis	Intro to Yosys / DC, area reports	SDC constraints, timing analysis	Multi-corner STA, timing closure
Physical Design	CMOS layout basics, Magic tool	Floorplan, placement, OpenROAD	CTS, routing, DRC/LVS sign-off
Verification	Directed testbench, waveform debug	Coverage-driven verification, SVA	UVM environment, functional closure
Tools & Scripting	LTspice, ModelSim basics	PrimeTime, Python/Tcl automation	OpenLane end-to-end, Calibre sign-off

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

PROGRAM ROADMAP

Your Path After Completing the Course

Completing this 12-week program is your launchpad — not your finish line. Here is the recommended roadmap to maximize your career outcomes and continue growing as a VLSI professional after graduation.

1

Month 1 After Course — Portfolio & Applications

Publish your capstone project on GitHub. Document your RTL design, physical design screenshots, and DRC/LVS reports. Apply to 10–15 targeted VLSI roles using the skills map as your resume guide.

2

Month 2–3 — Specialization Deep Dive

Choose your track: RTL Design, Physical Design, or Verification. Go deeper — complete one advanced resource (e.g., Synopsys training, Udemy STA course, or SystemVerilog/UVM textbook) to strengthen your specialization.

3

Month 4–6 — FPGA Prototyping Practice

Build 2–3 additional FPGA projects using Xilinx or Intel boards. Real hardware experience significantly differentiates candidates. Target internships, contract roles, or junior positions in parallel.

4

Month 6+ — First Industry Role

Target junior positions: RTL Design Engineer, DV Engineer, or Physical Design Analyst. Leverage mentor connections, alumni network, and LinkedIn outreach. Most graduates are interview-ready by this point.

5

Year 2–3 — Senior Readiness

Earn Synopsys/Cadence certifications, contribute to open-source VLSI projects (OpenROAD, CHIPS Alliance), and build expertise in a specific domain (AI chips, automotive, RF). The path to senior engineer accelerates significantly with structured early experience.

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

KEY TAKEAWAYS

What Makes This Course Different

End-to-End Flow Coverage

Most courses teach concepts in isolation. This program takes you through the **complete VLSI design flow** — from CMOS physics to GDSII tapeout — exactly the way industry teams work.

Live Mentoring Every Week

You are never learning alone. Every week includes a **live 1:1 or small-group mentoring session** with an industry expert — for doubt resolution, design reviews, and career guidance.

Real Tools, Real Workflows

Hands-on exercises use **industry-standard EDA tools** (and open-source equivalents), so your skills transfer directly to a professional environment from day one on the job.

12

Structured Weeks

Three progressive phases with clear milestones

3

Capstone Projects

One per phase — portfolio-ready deliverables

6+

EDA Tools

Industry and open-source tools covered hands-on

3

Industry Cases

Detailed real-world scenarios with measurable impact

EDVANTA

EDVANTA

Ignite your growth, inspire your mind

Ready to Build Your VLSI Career?

The semiconductor industry is growing faster than its talent pipeline. Companies are actively hiring engineers who can combine strong fundamentals with practical tool experience — and that is exactly what this program delivers.

In 12 weeks, you will go from building your first CMOS circuit to taping out a complete digital design. You will have a verified portfolio, industry-aligned skills, and a professional network built through live mentoring sessions. **Your first chip starts here.**

Start Any Cohort

New batches open monthly. Weekend-friendly schedule designed for working professionals and students.

Certificate of Completion

Industry-recognized certificate upon passing the capstone project and meeting attendance requirements.

Mentor Network Access

Lifetime access to the alumni community and quarterly industry panels with senior VLSI professionals.

Next Step: Review the full course syllabus, confirm your EDA tool access (OpenLane setup guide provided on enrollment), and join the cohort Slack workspace. Your mentor will reach out within 48 hours of enrollment to schedule your Week 1 onboarding session.

EDVANTA